IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Hui-Ling Lou et al.
Case: 13-13
Serial No.: 09/390,389
Filing Date: September 3, 1999
Group: 2631
Examiner: Kevin Michael Burd

Title: Multiplier-Free Methods and Apparatus for Signal Processing in a Digital Communication System

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SUPPLEMENTAL APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Appeal Brief is submitted in response to the Office Action dated July 29, 2004 in the above-referenced application, in which the Examiner reopened prosecution in response to the Appeal Brief filed May 11, 2004.

Applicants have submitted concurrently herewith a response to the Office Action, requesting reinstatement of the appeal.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

STATUS OF CLAIMS

The present application was filed on September 3, 1999 with claims 1-25. Claims 6, 7, 17, 18, 23 and 25 were canceled in an amendment filed on March 7, 2003. Claims 1-5, 8-16, 19-22 and 24 are currently pending in the present application. Claims 1, 12 and 24 are the independent claims.

Claims 1-5, 8-16, 19-22 and 24 stand rejected under 35 U.S.C. §112, second paragraph. Claims 1-4, 10-15, 21, 22 and 24 stand rejected under 35 U.S.C. §102(e). Claims 5, 8, 9, 16, 19 and 20 are indicated as being allowable if rewritten to overcome the §112 rejection. Claims 1-5, 8-16, 19-22 and 24 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the appealed rejection.

SUMMARY OF INVENTION

The present invention is directed to arrangements for processing information in a receiver of a digital communication system. A signal processing operation is applied to a sequence of transmitted symbols, where each of the symbols represents a particular number of information bits and corresponds to a point in a first modulation constellation. The first modulation constellation corresponds to a rotated version of a second modulation constellation. The signal processing operation utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols. More specifically, the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

Illustrative embodiments of the invention are described in the specification at, for example, page 7, line 20, to page 10, line 25, and are shown in the computational structures in FIGS. 3-6, 8, 9, 11, 13, 14 and 16 of the drawings.

The claimed arrangements provide important advantages over conventional techniques. For example, as indicated in the specification at page 3, lines 9-14, and page 4, lines 1-9, the invention in an illustrative embodiment can eliminate or substantially reduce the number of required

multipliers, and thus "significantly reduces the complexity and delay associated with the corresponding signal processing circuitry."

ISSUES PRESENTED FOR REVIEW

1. Whether claims 1-5, 8-16, 19-22 and 24 are indefinite under 35 U.S.C. §112, second paragraph.

2. Whether claims 1-4, 10-15, 21, 22 and 24 are anticipated under 35 U.S.C. §102(e) by U.S. Patent No. 6,611,567 (hereinafter "Balakrishnan").

GROUPING OF CLAIMS

With regard to Issue 1, claims 1-5, 8-16, 19-22 and 24 stand or fall together.

With regard to Issue 2, claims 1-4, 12-15 and 24 stand or fall together, claims 10 and 21 stand or fall together, and claims 11 and 22 stand or fall together.

ARGUMENT

Issue 1

The Examiner argues that the limitations in claims 1, 12 and 24 relating to the "at least one selector" are indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully traverse. Independent claim 1 is directed to a method of processing information in a receiver of a digital communication system. The claim includes, among other limitations, the following limitations denoted (a) and (b) herein for ease of discussion:

> (a) a signal processing operation applied to a sequence of transmitted symbols utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols; and
>
> (b) the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the

element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

The Examiner more specifically argues that the above limitations are unclear because "a product is defined as the number of [sic] quantity obtained by multiplying two or more numbers together." Applicants respectfully submit that the limitations in question are not inconsistent with the product statement proffered by the Examiner. Limitation (a) states that a signal processing operation applied to a sequence of transmitted symbols utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols, and the selector is more particularly described in limitation (b). An illustrative example of a selector meeting the claim limitations is shown in FIG. 3, and described as follows at page 7, lines 20-24, with emphasis supplied:

> FIG. 3 illustrates a basic selector structure for implementing the above-noted selection operation, i.e., the selection process for a QPSK modulation that leads to a complex multiplication according to the table of FIG. 2 and Equations (5) through (8) above. The basic selector structure includes inverters 10-1 and 10-2, and switches 12-1 and 12-2, interconnected as shown. As is apparent from FIG. 3, the selection operation does not require any multiplication or addition.

A number of other examples of types of selectors meeting the claim limitations are also described in the specification.

Accordingly, it is clear that limitations (a) and (b) of claim 1, and more particularly the "at least one selector" referred to in the claim, are not in any way inconsistent with the product statement proffered by the Examiner. The other independent claims include selector limitations similar to those of claim 1, and are also believed to be compliant with §112.

For the reasons identified above, the §112 rejection is believed to be improper, and should be withdrawn.

Issue 2

The Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully submit that the Examiner has failed to establish anticipation of claims 1-4, 10-15, 21, 22 and 24 by the Balakrishnan reference.

Applicants initially note that the Balakrishnan reference utilized by the Examiner in formulating the §102(e) rejection is commonly assigned with the present application. Although the present application, as an application filed on September 3, 1999, is not currently entitled to the benefit of 35 U.S.C. §103(c), Applicants note that the subject matter of the Balakrishnan reference and the claimed invention were, at the time the invention was made, owned by or subject to an obligation of assignment to the same person, namely, Lucent Technologies Inc. Both applications were subsequently assigned by Lucent Technologies to Agere Systems. Therefore, should the present application later become entitled to the benefit of §103(c), through the filing of a continuation or otherwise, the Balakrishnan reference will not be available for use as a §103(a) reference. See MPEP §706.02(l).

As indicated above, independent claim 1 is directed to a method of processing information in a receiver of a digital communication system. The claim includes, among other limitations, the previously-noted limitations (a) and (b).

The Examiner in formulating the §102(e) rejection argues that limitations (a) and (b) of claim 1 are met by Balakrishnan. Applicants respectfully disagree. Claim 1 calls for operations associated with the processing of information in a receiver of a digital communication system. The arrangements in Balakrishnan relied on by the Examiner are described therein as being utilized for pulse shaping in conjunction with transmission of modulated symbols. This pulse shaping apparently occurs prior to transmission over a bandlimited channel. See, for example, column 1,

lines 52-66, of Balakrishnan. Accordingly, there appears to be no teaching regarding the claimed signal processing operations, which are described as being performed in a receiver of a communication system. Also, as indicated in limitations (a) and (b) of claim 1, the claim calls for utilizing at least one selector to compute a product of a channel estimate and a given transmitted symbol, where the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol. The arrangements relied on by the Examiner fail to meet these particular limitations, in that there is apparently no mention of the use of a selector in conjunction with a channel estimate.

Accordingly, it is believed that the Examiner has failed to establish anticipation of claim 1 by Balakrishnan.

Independent claims 12 and 24 include limitations similar to those of claim 1, and are therefore believed to be allowable for substantially the same reasons identified above with regard to claim 1.

Dependent claims 2-4, 10, 11, 13-15, 21 and 22 are believed allowable for at least the reasons identified above with regard to their respective independent claims. Moreover, these claims are believed to define additional separately-patentable subject matter relative to the prior art references of record.

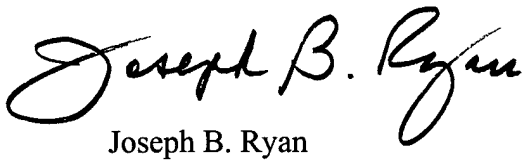
With regard to dependent claims 10 and 21, each of these claims generally specifies that the signal processing operation comprises a multi-stage multiplication operation implemented without multiplication operations, wherein each stage of the multi-stage operation corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage. The Examiner relies on column 3, lines 46-51, of Balakrishnan, but the relied-upon portion of the reference fails to meet the particular limitations of claims 10 and 21. Thus, it is believed that these claims are not anticipated by Balakrishnan.

With regard to dependent claims 11 and 22, these claims call for implementation of a selector-based signal processing operation and a selector-based signal processing circuit, respectively, utilizing a multi-stage hierarchical adder tree without multiplication operations. Again, the Examiner relies on column 3, lines 46-51, of Balakrishnan, but the relied-upon portion fails to

meet the particular limitations of claims 11 and 22. Thus, it is believed that these claims are not anticipated by Balakrishnan.

In view of the above, Applicants believe that claims 1-5, 8-16, 19-22 and 24 are in condition for allowance, and respectfully request withdrawal of the §112 and §102(e) rejections.

Respectfully submitted,



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APPENDIX

1. (Amended) A method of processing information in a receiver of a digital communication system, the method comprising the step of:

applying a signal processing operation to a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation, the first modulation constellation corresponds to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

the signal processing operation utilizing at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols;

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

2. (Original) The method of claim 1 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

3. (Original) The method of claim 1 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

4. (Original) The method of claim 1 wherein the second modulation constellation comprises one of a PSK constellation and a QAM constellation.

5. (Original) The method of claim 1 wherein the signal processing operation comprises at least one of a finite impulse response (FIR) filtering operation, a Least-Mean-Squares (LMS) estimation operation, and a Maximum-Likelihood (ML) sequence detection operation using a Viterbi algorithm.

6. (Canceled)

7. (Canceled)

8. (Amended) The method of claim 1 wherein the selector comprises first and second switches and first and second add/subtract units, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate for application to a corresponding one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

9. (Original) The method of claim 8 wherein an FIR filter operation is implemented using the selector by including feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

10. (Original) The method of claim 1 wherein the signal processing operation comprises a multi-stage multiplication operation implemented without multiplication operations, wherein each

stage of the multi-stage operation corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

11. (Original) The method of claim 1 wherein the signal processing operation is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

12. (Amended) An apparatus for use in processing information in a receiver of a digital communication system, the apparatus comprising:

a signal processing circuit for processing a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation, the first modulation constellation corresponds to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

wherein the signal processing circuit comprises at least one selector configured to compute a product of a channel estimate and a given one of the transmitted symbols; and

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

13. (Original) The apparatus of claim 12 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

14. (Original) The apparatus of claim 12 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

15. (Original) The apparatus of claim 12 wherein the other modulation constellation comprises one of a PSK constellation and a QAM constellation.

16. (Original) The apparatus of claim 12 wherein the signal processing circuit comprises at least one of a finite impulse response (FIR) filter, a Least-Mean-Squares (LMS) estimator, and a Maximum-Likelihood (ML) sequence detector implemented using a Viterbi algorithm.

17. (Canceled)

18. (Canceled)

19. (Amended) The apparatus of claim 12 wherein the selector comprises first and second switches and first and second add/subtract units, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate for application to a corresponding one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

20. (Original) The apparatus of claim 19 wherein the signal processing circuit comprises an FIR filter implemented using the selector configured with feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

21. (Original) The apparatus of claim 12 wherein the signal processing circuit comprises a multi-stage circuit implemented without multiplication operations, wherein each stage of the multi-stage circuit corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

22. (Original) The apparatus of claim 12 wherein the signal processing circuit is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

23. (Canceled)

24. (Amended) A method of processing information in a transmitter of a digital communication system, the method comprising the step of:

generating a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation generated by applying a predetermined rotation to a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

the transmitted symbols being configured such that a signal processing operation applied in a corresponding receiver of the system is implementable utilizing at least one selector configured to compute a product of a channel estimate and a given one of the transmitted symbols;

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

25. (Canceled)